MONOLITHIC GALLIUM ARSENIDE I-Q DEMODULATOR

V.P O'Neil*, C.Ryan*, C. Weitzel+

*Motorola, Inc., Government Electronics Group
Communications Research Facility
75 West Olive Ave.
Gilbert, AZ 85234

+Motorola, Inc., Semiconductor Product Sector
Semiconductor Research and Development Laboratories
5005 E. McDowell Rd.
Phoenix, AZ 85008

ABSTRACT

The monolithic gallium arsenide demodulator described herein demodulates the in-phase (I) and quadrature (Q) components of two signal channels on carriers identical in frequency but in quadrature phase relationships. The present demodulator is shown to be closely matched because of close matching of component parameters achieved by fabricating the entire demodulator on a single gallium arsenide chip. The demodulator can be developed to replace diode ring demodulators to obtain the following advantages:

* Less local oscillator power required
* Easier to match single ended inputs
* Better linearity at low signal levels
* Unilateral signal flow
* Less circuit "tweaking" required

In addition, the basic structure will lend itself to the development of a monolithic image rejection mixer with similar advantages.

THEORY

The monolithic chip consists of two interconnected four quadrant multipliers of the gain control type described by Ryan et. al. [1,2] as shown in Figure 3. Each of the multipliers has a small signal response which may be represented as:

$$(I_1 - I_2) = \frac{\sqrt{I_{SS} I_{DSS}}\,(V_1 - V_2)(V_3 - V_4)}{2 V_P^2}$$

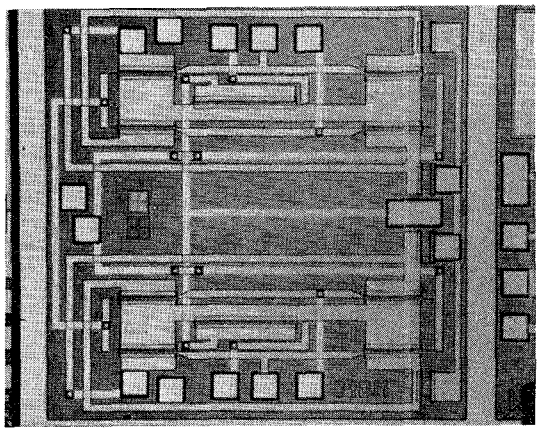

Figure 1 I-Q Demodulator Chip

When the multiplier is used as a demodulator with high level injection applied in the form

$$(V_1 - V_2) = V_0 \sin(\omega t)$$

then the conversion transconductance becomes:

$$g_{mc} = \frac{(I_1 - I_2)}{(V_3 - V_4)} = \frac{V_0 \sqrt{I_{SS} I_{DSS}}}{\pi V_P^2}$$

For the present demodulator important parameters are transconductance gain and phase matching. Transconductance variations among FET's on separate wafers have been observed to have transconductance variations as high as plus or minus 30 percent. This ratio of error in transconductance translates directly into a gain mismatch of 8dB between multipliers from different wafers. However, as the variation in transconductance on a single chip is much

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smaller (5% is typical) then the variation in gain is also expected to be smaller, approximately 1dB between two matched demodulators on the same chip. This close matching of gain and phase through the demodulators is essential to further signal processing.

Similarly, the first order approximation to the phase shift through a single multiplier cell is

$$\phi = TAN^{-1}\left(\frac{F}{F_T}\right)$$

Since error in F_t can be related primarily to the accuracy of the gate photoresist etching through the relation[5]

$$F_T = \frac{9.4\ GHZ\text{-}MICRON}{L_G} = \frac{K}{L_G}$$

then

$$\frac{d\phi}{dL_G} = \frac{180}{\pi}\left(\frac{1}{\frac{F^2L_G^2}{K^2} + 1}\right)\frac{F}{K}$$

The wafer to wafer variation in the length of the gate due to normal photoresist variations has been observed to be approximately 20%, while the variation between FET's on the same chip is so small as to be difficult to measure. Figure 2 shows the calculated variation in phase shift difference through two multipliers differing in gate length but otherwise identical, plotted versus nomralized frequency with gate length matching as a parameter. The larger error is calculated for an assumed mismatch of 20% in gate length, while the smaller error is for an assumed mismatch of 5%. The close matching of the phase difference makes the circuit components other than the demodulator become the limiting performance factors.

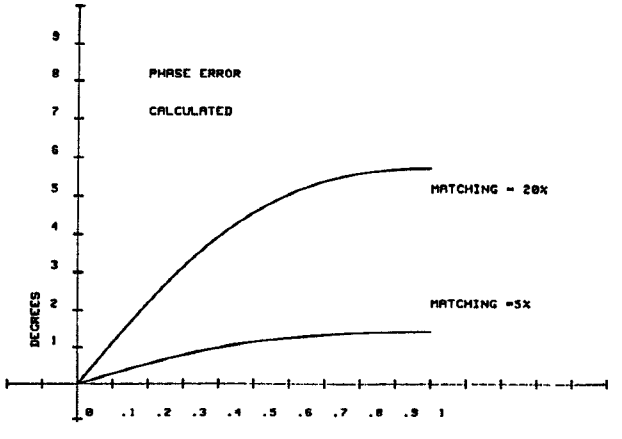

Figure 2 Phase Error vs Normalized Frequency F/FT

FABRICATION

The starting material for the process is epitaxial GaAs grown by $AsCl_3$ VPE on semi-insulating GaAs substrate with an interposed high resistivity buffer layer. The doping density of the active layer is 2.5×10^{17} cm^{-3}. The first photolithographic step defines the FET and resistor areas. Mesas are etched with a dilute solution of H_2SO_4 and H_2O_2. The next photolithographic step defines the ohmic contacts for the FETs and epitaxial resistors. After evaporation, the unwanted AuGe/Ni is removed by lift-off. The contacts are alloyed at 450°C for 2.75 minutes in forming gas. The first half of the process is completed by defining the first-level metal, evaporating TiPtAu (7500 A) and lifting off the unwanted metal. At this point in the process the FETs and resistors can be electrically characterized. A 1 micron polyimide layer is applied and patterned to separate the two metal layers.

Plasma silicon nitride is deposited on the wafer to a thickness of about 2000 A. Vias and bond pads are defined using positive photoresist and exposed silicon nitride is then etched in a CF_4 plasma. The process is completed by defining the second-level interconnects, evaporating TiAu (9000 A), and lifting off unwanted metal.

The typical d.c. characteristics of 1 mm wide FETs with L_g = 1 micron and L_{SD} = 4 microns were V_p = -3.0 V, I_{DSS} = 210 ma, G_M (I_{DSS}) = 100 mS, and G_M (40 ma) = 70 mS. The capacitance between first-level and second-level metal crossover is 0.03 femtofarads/micron^2.

PREDICTED PERFORMANCE

The complete circuit of the I-Q demodulator is shown in Figure 3. The FET's used have the following nominal parameters and operating conditions:

Z = 150 microns
L = 1 micron
I_{dss} = 22 mA
F_t = 12 GHz
I_{ss} = 7 mA
V_p = -2.5 volts

The multiplier described herein was tested in 50 ohm system using unmatched single ended inputs and outputs. The calculated gain in such a system is given by:

$$G_c = 20\ LOG\left(g_{mc}\right)(50\Omega)$$
$$= 20\ LOG\left(\frac{50}{\pi V_p}\sqrt{I_{DSS}I_{SS}}\right) = -29dB$$

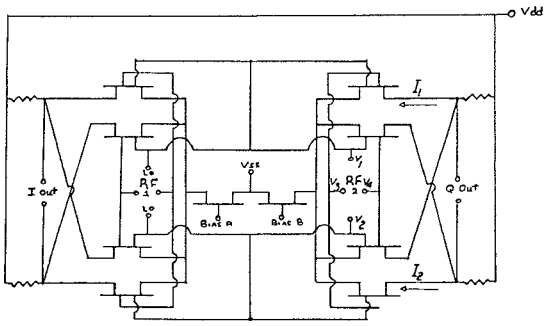

Figure 3 Complete Demodulator Schematic

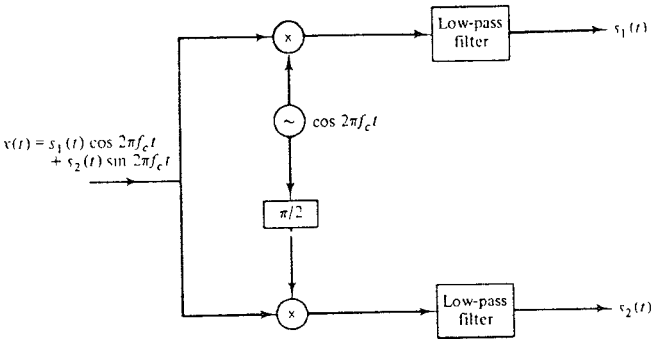

Fig. 4. I-Q Demodulator Test Circuit

This simple first-order calculation gives results in close agreement with simulation of the circuit using the SPICE simulation software package. Much greater conversion power gain could be obtained with proper matching of input and output impedances; accomplishment of this potential by active and passive impedance transformation techniques will be an object of future investigation.

MEASURED PERFORMANCE

The test system is shown in Figure 4, the outputs s1(t) and s2(t) are expected to be two tones of equal frequency and quadrature phase relationship, and related to the input amplitude by the gain relation developed above. The measurements were made at nominal input frequencies of 2500,3000 MHz and 2500 GHz over at IF frequencies of 0-4000 MHz. Measurements at higher frequencies were complicated by the fact that the prototype multiplier has 14 pins including the bias points, and this package did not have satisfactory high frequency characteristics to allow proper measurements. The measurements of gain and phase difference between the two channels are plotted in Figure 5 through 10 versus the difference between the local oscillator and RF frequencies. The measurements included all sources of error including the demodulators and indicate the contribution of the demodulators to the total error is small over the intermediate frequency range.

SUMMARY

The gallium arsendide I-Q demodulator described above has demonstrated the expected advantages of monolithic devices in the maintenance of close gain and phase matching between the I and Q channels.

The results obtained indicate that the device can be developed to replace diode ring mixers now used in this application to obtain the following advantages:

* Less circuit "tweaking" required to obtain the required matching
* Easier to match single ended FET inputs and outputs
* Wider dynamic range due to better small signal linearity
* Unilateral signal flow through the multipliers
* Higher gain through the circuit than diode ring demodulators
* Less RF power required at the local oscillator ports
* Can be incorporated as a cell into more complex monolithic signal processing circuits

FUTURE WORK

Several areas of investigation are expected to result in improved performance of the above demodulator:

* The extension of the performance by the use of .5 micron FET's is to be investigated. The advantages of monolithic matching should become more pronounced as the gate length is shortened because of the greater difficulty of maintaining tight tolerances in the photoresist processes.

* Impedance matching networks on the input and outputs will improve the gain of the demodulators and reduce the local oscillator power requirement.

* At operating frequencies in excess of 8 GHz, the possibility of integrating the quadrature coupler[3] and impedance matched networks[4] on the chip becomes a real possibility.

* Reduction of the number of pins by on-chip biasing networks can reduce the number of pins required, making higher frequency packaging attainable.

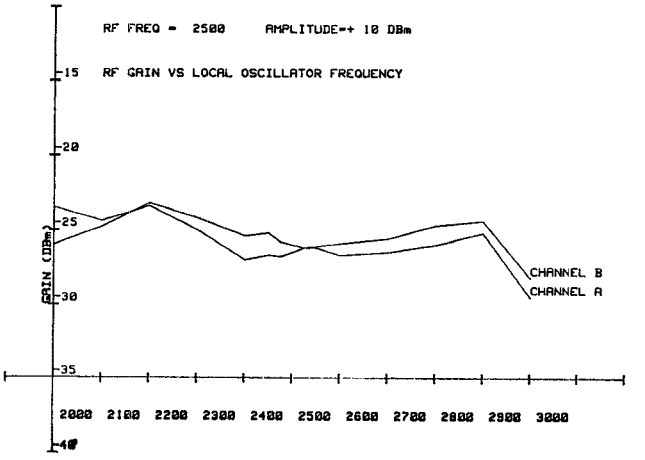

Figure 5

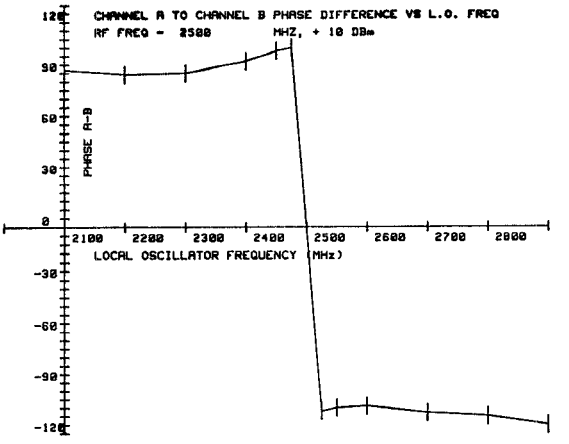

Figure 6

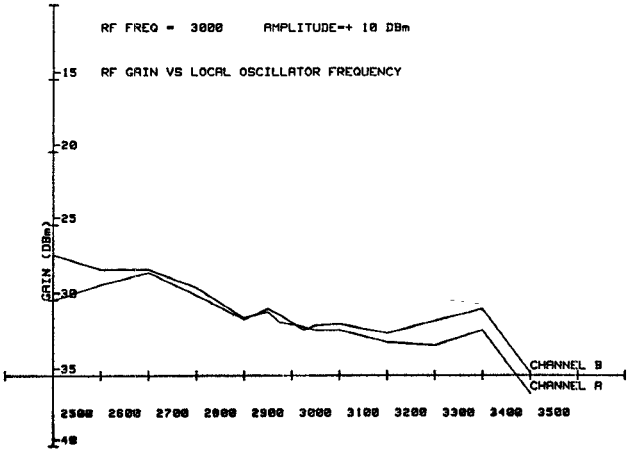

Figure 7

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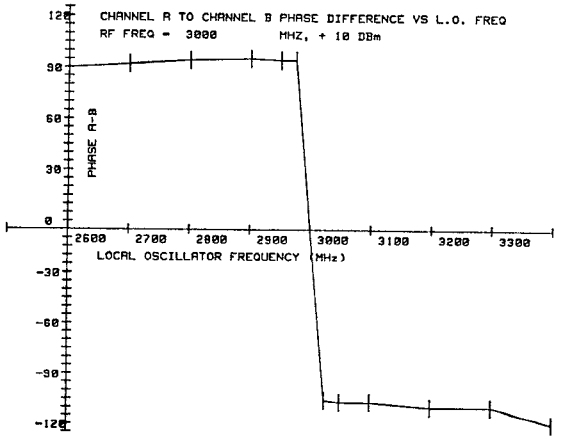

Figure 8

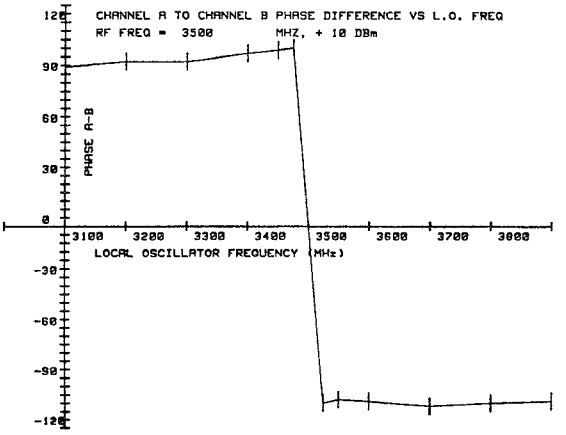

Figure 10

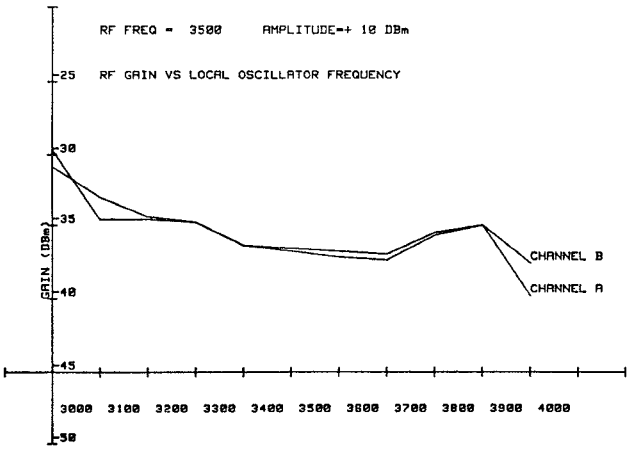

Figure 9